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Claims

[c1] 1.A multi-chip package comprising:
an upper arrayed package having a two-dimensional array of electrical connections with at least four rows and four columns;
a lower arrayed package having a two-dimensional array of electrical connections with at least four rows and four columns;
an intermediate adapter card between the upper arrayed package and the lower arrayed package;
a bottom adapter card between the lower arrayed package and a circuit board;
first metal contacts on a first surface of the intermediate adapter card, the first metal contacts disposed in an array to match the two-dimensional array of electrical connections of the upper arrayed package;
lead frame pins that wrap around edges of the intermediate adapter card from the first surface to below a second surface of the intermediate adapter card;
first metal traces on the first surface of the intermediate adapter card to electrically connect the first metal contacts to the lead frame pins;
peripheral pads around a periphery of a first surface of

the bottom adapter card, the peripheral pads disposed to make electrical contact with the lead frame pins from the intermediate adapter card;

second metal contacts on the first surface of the bottom adapter card, the second metal contacts disposed in an array to match the two-dimensional array of electrical connections of the lower arrayed package;

second metal traces on the first surface of the bottom adapter card to electrically connect the second metal contacts to the peripheral pads; and

final bonding pads on a second surface of the bottom adapter card, for making electrical contact with the circuit board,

whereby the upper arrayed package and the lower arrayed package are stacked together using the intermediate adapter card and the bottom adapter card to route arrayed electrical connections to the periphery.

[c2] 2.The multi-chip package of claim 1 further comprising:

vias through the bottom adapter card to connect the peripheral pads on the first surface to the final bonding pads on the second surface of the bottom adapter card.

[c3] 3.The multi-chip package of claim 2 wherein the two-dimensional array of electrical connections of the upper arrayed package and of the lower arrayed package are solder balls, pads, leads, or pins in an array.

[c4] 4.The multi-chip package of claim 3 wherein the upper arrayed package and the lower arrayed package are Ball Grid Array (BGA) packages.

[c5] 5.The multi-chip package of claim 4 wherein the upper arrayed package and the lower arrayed package have a same footprint of the two-dimensional array of electrical connections with at least four rows and four columns.

[c6] 6.The multi-chip package of claim 5 wherein the upper arrayed package and the lower arrayed package are memory chips.

[c7] 7.The multi-chip package of claim 3 further comprising:
a molding attached to the second surface of the intermediate adapter card;
wherein the lead frame pins are shaped by the molding.

[c8] 8.The multi-chip package of claim 3 further comprising:
a third arrayed package having a two-dimensional array of electrical connections with at least four rows and four columns;
an upper intermediate adapter card between the third arrayed package and the upper arrayed package;
third metal contacts on a first surface of the upper intermediate adapter card, the third metal contacts disposed in an array to match the two-dimensional array of elec-

trical connections of the third arrayed package;
second lead frame pins that wrap around edges of the upper intermediate adapter card from the first surface to below a second surface of the upper intermediate adapter card;
third metal traces on the first surface of the upper intermediate adapter card to electrically connect the third metal contacts to the second lead frame pins; and
second peripheral pads around a periphery of a first surface of the intermediate adapter card, the second peripheral pads disposed to make electrical contact with the second lead frame pins from the upper intermediate adapter card,
wherein three arrayed packages are stacked together.

[c9] 9.A stacked Ball Grid Array (BGA) package comprising:
a top BGA device having an array of first contacts on a lower surface;
a bottom BGA device having an array of second contacts on a lower surface;
an intermediate adapter card having a top surface facing the lower surface of the top BGA device, and a lower surface facing the bottom BGA device;
a first array of metal contacts on the top surface of the intermediate adapter card for electrically contacting the array of first contacts of the top BGA device;

intermediate metal traces on the intermediate adapter card that connect to the first array of metal contacts;
peripheral connectors, electrically connected to the intermediate metal traces, disposed around edges of the intermediate adapter card;
a bottom adapter card having a top surface facing the lower surface of the bottom BGA device, and a lower surface facing a mounting board;
a second array of metal contacts on the top surface of the bottom adapter card for electrically contacting the array of second contacts of the bottom BGA device;
peripheral pads on the top surface of the bottom adapter card, for contacting the peripheral connectors of the intermediate adapter card;
bottom metal traces on the bottom adapter card that connect to the second array of metal contacts to the peripheral pads;
final bonding pads on the bottom adapter card and electrically connected to the bottom metal traces, for soldering to the mounting board.

[c10] 10.The stacked BGA package of claim 9 wherein the bottom metal traces on the bottom adapter card are formed on the top surface of the bottom adapter card.

[c11] 11.The stacked BGA package of claim 10 further comprising:

vias through the bottom adapter card for connecting the bottom metal traces on the top surface of the bottom adapter card to the final bonding pads on the lower surface of the bottom adapter card.

[c12] 12.The stacked BGA package of claim 11 wherein the peripheral connectors of the intermediate adapter card are soldered to the peripheral pads of the bottom adapter card to make electrical connections.

[c13] 13.The stacked BGA package of claim 9 wherein the intermediate metal traces on the intermediate adapter card are formed on the top surface of the intermediate adapter card.

[c14] 14.The stacked BGA package of claim 9 further comprising the mounting board, wherein the mounting board is a printed-circuit board (PCB), a motherboard, or a memory module substrate.

[c15] 15.The stacked BGA package of claim 9 wherein the top BGA device and the bottom BGA device are each packaged integrated circuits.

[c16] 16.The stacked BGA package of claim 15 wherein the array of first contacts has at least four columns and at least four rows;
wherein the array of second contacts has at least four

columns and at least four rows.

[c17] 17.The stacked BGA package of claim 15 wherein the peripheral connectors are lead frame pins.

[c18] 18.The stacked BGA package of claim 16 further comprising:
a molding under the lower surface of the intermediate adapter card, the molding for shaping the peripheral connectors into a U shape.

[c19] 19.A stacked-chip assembly for mounting on a mounting board comprising:
upper arrayed package means, having a two-dimensional array of electrical connections with at least four rows and four columns, for connecting an enclosed integrated circuit through the two-dimensional array of electrical connections;
lower arrayed package means, having a two-dimensional array of electrical connections with at least four rows and four columns, for connecting an enclosed integrated circuit through the two-dimensional array of electrical connections;
intermediate adapter card means for interfacing to the upper arrayed package means;
bottom adapter card means for interfacing between the lower arrayed package means and a circuit board;

first metal contact means, on a first surface of the intermediate adapter card means, for matching a footprint of the two-dimensional array of electrical connections of the upper arrayed package means;

lead frame means for wrapping around edges of the intermediate adapter card means from the first surface to below a second surface of the intermediate adapter card means;

first metal means, on the first surface of the intermediate adapter card means, for electrically connecting the first metal contact means to the lead frame means;

peripheral pad means, disposed around a periphery of a first surface of the bottom adapter card means, for making electrical contact with the lead frame means from the intermediate adapter card means;

second metal contact means, on the first surface of the bottom adapter card means, for matching a footprint of the two-dimensional array of electrical connections of the lower arrayed package means;

second metal means, on the first surface of the bottom adapter card means, for electrically connecting the second metal contact means to the peripheral pad means; and

final bonding pad means, on a second surface of the bottom adapter card means, for making electrical contact with the circuit board,

whereby the upper arrayed package means and the lower arrayed package means are stacked together using the intermediate adapter card means and the bottom adapter card means to route arrayed electrical connections to the periphery.

[c20] 20.The stacked-chip assembly of claim 19 wherein the upper arrayed package means is a Ball Grid Array (BGA) package; and
wherein the lower arrayed package means is a BGA package.